CHUN HOK HO

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Working/Research Experience

- **SK Hynix Memory Solutions (San Jose, CA)** – Staff Design Engineer **Mar 2011 – Present**
  - Design Solid State Drive (SSD) controller on mobile, client and enterprise systems.
  - Design system performance model for SSD controller.
  - Design traffic simulator for SSD controller.
  - Design and maintain data recovery IP (RAID) for SSD controller.
  - Design and maintain power management IP for mobile SSD controller.
  - Define next generation SSD controller architecture.
  - Develop analog simulation model for mixed-signal verification.
  - Refine verification flow and speedup the compilation time by 5 times.
  - Refine design database structure, enhance database integrity and performance.
  - Develop scripts to automate lint checking and ECO process.

- **Hong Kong Polytechnic University (Hong Kong)** – Post-Doc Researcher **Jan 2010 – Oct 2010**
  - Researched DSP and financial applications using reconfigurable technology.
  - Designed low-power DSP platform for portable embedded devices.
  - Analyzed American Options and Asian Options algorithms with MATLAB.
  - Designed accelerators for pricing American and Asian Options on Xilinx FPGA and Nvidia GPU devices.
  - Advised PhD/MSc students on general programming and circuit debugging techniques.

- **Imperial College (London, UK)** – Ph. D **Oct 2005 – Jan 2010**
  - Invented Floating Point FPGA architectures. Floating point circuits perform 4 times faster and were 25 times smaller compared with existing FPGAs.
  - Designed compiler and technology mapper (in Perl/Java) enabling applications compile to Floating Point FPGA.
  - Designed proof-of-concept layout using SoC design flow.
  - Implemented DSP applications, medical imaging applications, physics simulations and financial engineering problems on Floating Point FPGAs.
  - Designed reconfigurable logic embedded into SoC for post-silicon debugging.
  - Invented a novel methodology to model FPGA architecture, including speed, area and power, in comparison with Xilinx/Altera devices.
  - Designed Perl/Tcl scripts to design parameterized floating point unit in ASIC.
  - Published 10 technical papers and 2 journal papers.
  - Received 3 best paper awards on various academic conferences.

- **Xilinx Inc. (San Jose, CA)** – Research Intern **Feb 2007 – Aug 2007**
  - Participated in CHiMPS development, a tool to allow software developers to program hybrid CPU-FPGA platforms with C language.
  - Designed memory hierarchy for CHiMPS circuits.

- Designed interface between the Berkeley Emulation Engine 2 board and CHiMPS circuits.
- Designed test plan for CHiMPS circuits.
- Evaluated floating point performance and memory throughput of CHiMPS circuits.

- **University of Hong Kong (Hong Kong)** – Research Associate **Jun 2005 – Sep 2005**
  - Designed novel acoustic DSP SoC system using FPGA to achieve real-time performance.
  - Analyzed and optimized various DSP algorithms (in C/Matlab) including echo-cancellation, and blind-signal separation.
  - Developed a cross-platform parameterized fixed point library (in C) on both embedded platform and desktop platform.
  - Implemented an optimized beamformer on FPGA platform, achieving 42 times speedup when compared with a single core PC system.
  - Implemented firmware on PowerPC to profile application performance.

- **Sengital Limited (Hong Kong)** – Electronic Engineer **Jun 2004 – Jun 2005**
  - First-batch of employees in a fast-paced start-up company.
  - Researched, developed, and commercialized technology around microelectromechanical systems (MEMS) with wireless system (Zigbee, Bluetooth).
  - Designed input devices for PC with MEMS technology similar to Wii controllers.
  - Designed mixed-signal PCB board (schematic capture and board layout).
  - Designed firmware (in assembly/C) on 4/8/16-bit MCU including PIC,TI MSP430.
  - Designed USB interface and the HID protocol.
  - Designed a light-weight wireless protocol stack.
  - Launched pilot production from initial design concepts in 8 months.

Education

- **Imperial College London** **Oct 2005 – Jan 2010**
  - Ph.D (Computing)
  - Thesis Title: *Customisable and Reconfigurable Platform for Optimising Floating Point Applications*
- **Chinese University of Hong Kong** **Aug 1998 – Jul 2003**
  - M. Phil. (Computer Science and Engineering)
  - Thesis Title: *Automatic Synthesis and Optimization of Floating Point Hardware*
  - B. Eng. (Computer Engineering)

Awards

- **Stamatis Vassiliadis Outstanding Paper Award**: Sep 2008.
- **Stamatis Vassiliadis Outstanding Paper Award**: Aug 2007.
- **Overseas Research Students Award**: Oct 2006 – Sep 2008.

Skills

- Hardware description languages – VHDL, Verilog, System Verilog
- Programming languages – Perl, Java, C/C++, C#, Matlab, shell script, CUDA, assembly

- EDA tools – Xilinx ISE, Quartus II, ModelSim, Synopsys Design Compiler, VCS, Power Compiler, Synplify Premier, Primetime, Cadence Encounter, RTL Compiler, Incisive Simulator, Protel DXP
- Web technology – HTML, PHP, JSP, AJAX, XML, JSON, Javascript
- Others – Latex, Haskell, SQL, Git

Selected Publications (Full-list http://www.chunhokho.com/pubs)

1. **C.H. Ho**, C.W. Yu, P.H.W. Leong, W. Luk and S.J.E. Wilton, "Floating Point FPGA: Architecture and Modelling". In *IEEE Transactions on Very Large Scale Integration Systems.*, vol. 17, no. 12, pp. 1709–1718, December 2009. **TVLSI Top 25 Downloaded Manuscripts in 2009, 2010.**
2. S.J.E. Wilton, **C.H. Ho**, B. Quinton, P.H.W. Leong and W. Luk, "A Synthesizable Datapath-Oriented Embedded FPGA Fabric for Silicon Debug Applications". In *ACM Transactions of Reconfigurable Technology and Systems*, 1(1):7:1–7:25, March 2008.
3. **C.H. Ho**, P.H.W. Leong, W. Luk and S.J.E. Wilton, "Rapid Estimation of Power Consumption for Hybrid FPGAs". In *Proceedings of Field Programmable Logic*, pp. 227–232, 2008. **Stamatis Vassiliadis outstanding paper award.**
4. K.F.C Yiu, **C.H. Ho**, N. Grbric, Y. Lu, X. Shi and W. Luk, "Reconfigurable Acceleration of Microphone Array Algorithms for Speech Enhancement". In Proceedings of Application-specific Systems, Architectures and Processors, pp. 209-214, 2008.
5. **C.H. Ho**, C.W. Yu, P.H.W. Leong, W. Luk and S.J.E. Wilton, "Domain-Specific FPGA: Architecture and Floating Point Applications". In *Proceedings of Field Programmable Logic*, pp. 196–201, 2007. **Stamatis Vassiliadis outstanding paper award.**
6. S.J.E. Wilton, **C.H. Ho**, P.H.W. Leong, W. Luk and B. Quinton, "A Synthesizable Datapath-Oriented Embedded FPGA Fabric". In *Proceedings of Fifteenth ACM/SIGDA International Symposium on FPGAs*, pp. 33–41, 2007.
7. **C.H. Ho**, K.F.C. Yiu, J. Huo and W. Luk, "Reconfigurable acceleration of robust frequency-domain echo cancellation". In *Proceedings of Engineering of Reconfigurable Systems and Algorithms*, pp. 184–190, 2006.
8. **C.H. Ho**, P.H.W. Leong, W. Luk, S.J.E. Wilton, S. Lopez-Buedo, "Virtual Embedded Blocks: A Methodology for Evaluating Embedded Elements in FPGAs". In *Proceedings of Field-Programmable Custom Computing Machines*, pp. 35–44, 2006.
9. G.L. Zhang, P.H.W. Leong, **C.H. Ho**, et. al, "Reconfigurable Acceleration for Monte Carlo based Financial Simulation". In *Proceedings of Field Programmable Technology*, pp. 215–222, 2005.
10. **C.H. Ho**, K.H. Tsoi, H.C. Yeung, Y.M. Lam, K.H. Lee, P.H.W. Leong, R. Ludewig, P. Zipf, A.G. Ortiz, M. Glesner, "Arbitrary Function Approximation in HDLs with application to the N-Body Problem". In *Proceedings of Field Programmable Technology*, pp. 84–91, 2003.
11. **C.H. Ho**, P.H.W. Leong, K.H. Lee, K.H. Tsoi, R. Ludewig, P. Zipf, A.G. Ortiz and M. Glesner, "*fly* - A Modifiable Hardware Compiler". In *Proceedings of Field Programmable Logic and Applications*, pp. 381–390, 2002.
12. **C.H. Ho**, M.P. Leong, P.H.W. Leong, J. Becker and M. Glesner,"Rapid Prototyping of FPGA based Floating-point DSP Systems". In *Proceedings of Rapid System Prototyping*, pp. 19–24, 2002.